REMARKS

Claims 1, 8 and 11 were rejected under 35 U.S.C. 112, first paragraph, as not enabling an "arbitrarily addressable storage means." The Examiner specifically points to the term "arbitrarily" while conceding that the specification does enable an addressable storage means. Applicant has amended claims 1, 8 and 11 to delete the term "arbitrarily."

Claim 32 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner notes that claim 32 depends from cancelled claim 6. Applicant has amended claim 32 to depend from claim 1.

Claims 1-3, 5, 7-12, 14-17 and 32-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman in view of Barnes, Gaudet and Wegner. Claims 15-23 and 36-38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman in view of Barnes and Gaudet.

Applicant has amended claims 1 and 8 to distinguish over the cited prior art.

Turning first to claim 1, Applicant claims "a processor configured to control the removal of packets from the store and the sending of the removed packets out through the plurality of output ports using the assigned destination pointers, wherein an order of packet removal from the store for sending out through the output ports depends on whether the output ports through which the removed packets are to be sent based on the assigned destination pointers are free to send out packets."

Applicant claims having the processor "control the removal of packets from the store and the sending of the removed packets out through the plurality of output ports using the assigned destination pointers." This does not appear to be taught by the cited prior art. Chapman uses output buffers 322/326 to hold packets prior to output through the output ports. The removal of packets from the buffers to send out through the output ports is NOT controlled using "assigned destination pointers" as claimed. The Examiner points to the routing table as meeting the claimed destination pointers. The routing table in Chapman, however, functions to control the loading of the packets into the output buffers 322/326 for subsequent transmission. This is different from the claimed invention wherein the destination pointers are used by the processor to control the actual sending of the packets out through the output ports.

Applicant further claims that the "order of packet removal from the store for sending out through the output ports depends on whether the output ports through which the removed packets are to be sent based on the assigned destination pointers are free to send out packets."

Applicant submits that this operation is not taught by the cited prior art. Chapman functions to load the output buffers 322/326 from memory 310, but there is no teaching or suggestion for conditioning this output buffer loading operation on whether output ports are free to send. In fact, the point of including an output buffer, as in Chapman, is to avoid having to test or condition an output operation on whether the output port is free to send the packet. By including an output buffer, as in Chapman, the system can function to support through-routing (by moving packets from memory 310 to buffer 322/326) without having to be concerned with whether the output port (at physical links 5/8) is free. The information is simply loaded into the output buffer and stored pending availability of the output port (physical link 5/8) to complete the transmission.

The Examiner has cited to Wegner which teaches a queuing mechanism that ensures that all ports are available before allowing a broadcast delivery. While this technique would facilitate a broadcast operation, the Wegner teachings are not implemented using the claimed invention. Wegner, like Chapman, fails to teach or suggest "a processor configured to control the removal of packets from the store and the sending of the removed packets out through the plurality of output ports using the assigned destination pointers, wherein an order of packet removal from the store for sending out through the output ports depends on whether the output ports through which the removed packets are to be sent based on the assigned destination pointers are free to send out packets."

Applicant further has amended claim 1 to recite "a store configured to hold packets of the input packet streams at addressable locations each identifiable by an address, said store being shared by all of said input ports and said output ports." The Examiner had previously pointed to the I/O FIFO buffers as meeting the claimed storage means. These buffers are not "shared by all of said input ports and said output ports" as claimed. Chapman teaches a memory 310 which is shared, but packets are not removed from memory 310 in the manner claimed by Applicant (see, discussion above).

In view of the foregoing, Applicant submits that claim 1 is patentable over the cited prior art.

Claim 8 has been amended similarly to claim 1, and Applicant asserts that claim 8 is patentable over the cited prior art for at least the same reasons as claim 1.

New claim 39 has been added. Claim 39 is a method claim having limitations similar to those presented in claims 1 and 8. Claim 39 is asserted to be patentable over the cited prior art for at least the same reasons as claims 1 and 8.

Applicant has amended claim 11 to distinguish over the cited prior art.

Applicant claims "providing an assignment data structure identifying for each input port identifier at least one intended output port to which the packet stream received at the input port is to be routed." The Examiner has previously identified a routing table in Chapman which maps destination addresses of incoming packets to output ports as meeting the claimed assignment data structure. Amended claim 11 emphasizes that the claimed "assignment data structure" establishes a relationship between an "input port identifier" and an "intended output port." Thus, the claimed relationship is not, as taught by Chapman, between a destination address and the output port, but rather between the ***input port identifier*** and the ***output port***. There is no suggestion in Chapman for this claimed relationship.

The Examiner further points to Gaudet and the monitoring of a source identification. The "source ID" in Gaudet concerns the "source port" of the packet, where that source port is contained within the packet header. This source port in Gaudet, however, is not the input port identifier as claimed, and thus Gaudet, like Chapman, does not teach or suggest an assignment data structure which establishes a relationship between the ***input port identifier*** and the ***output port***.

Amended claim 11 further recites "providing a packet allocation table comprising an array including a plurality of slots, each slot storing the input port identifier of the input port which received a packet from one of the packet streams and the address in the store where the received packet is held." The Examiner again points to the routing table in Chapman. However, the Chapman routing table associates destination addresses of incoming packets to output ports. The claimed packet allocation table, on the other hand, associates (in each slot) "the input port identifier" for the input port receiving the packet and the "address in the store where the received packet is held." The claimed invention is not met by Chapman. The Examiner's analysis of Chapman focuses on relationships between destination addresses read from the packet header and output port or delivery addresses. However, the packet header destination address is not the "input port identifier" claimed, and the delivery address is not the "address in the store" where the packet is held (or stored) after receipt. The Examiner further points to Gaudet, but as

discussed above Gaudet focuses on source port information, not the claimed input port identifier and its relationship to an address in memory where the packet is stored.

Claim 11 still further recites "using said assignment data structure identifying the intended output port for each input port identifier to assign each destination pointer to a slot of the packet allocation table based on the output port associated with the destination pointer and the input port identifier that is stored in the slot and identified with that output port by the assignment data structure." The Examiner again points to the routing table in Chapman. While this routing table drives the routing operation in Chapman, that routing operation differs from the claimed invention in that the destination pointer of the claimed invention is assigned based on the relationship between the input port identifier and the output port as specified by the assignment data structure. Chapman routes based on the relationship between the destination addresses read from the packet header and output port. There is no teaching or suggestion in Chapman for driving pointer operation based on an input port identifier and its association with one or more output ports.

The teachings of Gaudet and Wegner, which are also cited by the Examiner, do not suggest the claimed invention. Gaudet notes a source port identification within a packet header and Wegner teaches a queuing mechanism based on output port availability. Neither reference, however, teaching having the pointer for routing be assigned based on the stored relationship between the identifier of the input port where the packet was received and one or more output ports.

In view of the foregoing, Applicant submits that claim 11 is patentable over the cited prior art.

Claim 15 has also been amended to distinguish over the cited prior art.

Amended claim 15 recites "a matrix configured to map at least one input port identifier to at least one output port." The Examiner has previously identified a routing table in Chapman which maps destination addresses of incoming packets to output ports as meeting the claimed matrix. Amended claim 15 emphasizes that the claimed "matrix" establishes a mapped relationship between an "input port identifier" and an "output port." Thus, the claimed relationship is not, as taught by Chapman, between a destination address and the output port, but rather between the ***input port identifier*** and the ***output port***. There is no suggestion in Chapman for this claimed mapping relationship.

The Examiner further points to Gaudet and the monitoring of a source identification. The "source ID" in Gaudet concerns the "source port" of the packet, where that source port is contained within the packet header. This source port in Gaudet, however, is not the input port as claimed, and thus Gaudet, like Chapman, does not teach or suggest an assignment data structure which establishes a relationship between the ***input port identifier*** and the ***output port***.

Claim 15 further recites "a packet allocation table including a plurality of slots, each slot configured to associate an input port identifier for the input port at which a particular packet is received with the address location in the addressable memory where the particular packet is stored." The Examiner again points to the routing table in Chapman. However, the Chapman routing table associates destination addresses of incoming packets to output ports. The claimed packet allocation table, on the other hand, associates (in each slot) "the input port identifier" for the input port receiving the packet and the "address location in the addressable memory where the particular packet is stored." The claimed invention is not met by Chapman. The Examiner's analysis of Chapman focuses on relationships between destination addresses read from the packet header and output port or delivery addresses. However, the packet header destination address is not the "input port identifier" claimed, and the delivery address is not the "address location in the addressable memory" where the packet is held (or stored) after receipt. The Examiner further points to Gaudet, but as discussed above Gaudet focuses on source port information, not the claimed input port identifier and its relationship to an address in memory where the packet is stored.

Amended claim 15 also recites "an algorithm configured to control removal of the incoming packets from the memory to at least one output port, the algorithm assigning each destination pointer to a slot in the packet allocation table based on the output port associated with the destination pointer and the input port identifier within the slot of the packet allocation table and mapped to the output port by the matrix, wherein the packet at the address location within the slot of the packet allocation table assigned to the destination pointer is retrieved from the addressable memory and delivered to the output port associated with that destination pointer." The Examiner points to a packet discard operation in Chapman, but Applicant respectfully submits that this packet discard operation does not teach or suggest the specific operational functions of the claimed algorithm. In particular, Applicant claim that the algorithm controls the removal of packets from memory for output by assigning destination pointers. The Examiner has asserted that this operation is provided by the routing table in Chapman. While

this routing table drives the routing operation, that routing operation differs from the claimed invention in that the destination pointer of the claimed invention is assigned based on the relationship between the input port identifier and the output port as specified by the assignment data structure. Chapman routes based on the relationship between the destination addresses read from the packet header and output port. There is no teaching or suggestion in Chapman for driving pointer operation based on an input port identifier and its association with one or more output ports.

The teachings of Gaudet and Wegner, which are also cited by the Examiner, do not suggest the claimed invention. Gaudet notes a source port identification within a packet header and Wegner teaches a queuing mechanism based on output port availability. Neither reference, however, teaching having the pointer for routing be assigned based on the stored relationship between the identifier of the input port where the packet was received and one or more output ports.

In view of the foregoing, Applicant submits that claim 15 is patentable over the cited prior art.

Applicant has amended claim 36 to distinguish over the cited prior art.

Amended claim 36 recites "a matrix configured to map each input port receiving the input packet streams to one or more output ports for receiving the packets within those input packet streams." The Examiner has previously identified a routing table in Chapman which maps destination addresses of incoming packets to output ports as meeting the claimed matrix. Amended claim 36 emphasizes that the claimed "matrix" establishes a mapped relationship between an "input port" and an "output port." Thus, the claimed relationship is not, as taught by Chapman, between a destination address and the output port, but rather between the ***input port*** and the ***output port***. There is no suggestion in Chapman for this claimed mapping relationship.

The Examiner further points to Gaudet and the monitoring of a source identification. The "source ID" in Gaudet concerns the "source port" of the packet, where that source port is contained within the packet header. This source port in Gaudet, however, is not the input port as claimed, and thus Gaudet, like Chapman, does not teach or suggest an assignment data structure which establishes a relationship between the ***input port*** and the ***output port***.

Amended claim 36 further recites "an insertion circuit configured to insert into a header of each packet of the received input packet stream an input port identifier for the input port which received the input packet stream." This is a newly presented limitation added to claim 36.

Support for this limitation is provided by the insertion circuit block 7 of Figure 1. Applicant cannot find any teaching in the cited prior art for the claimed insertion circuit which inserts the "input port identifier for the input port which received the input packet stream" into the header of the received packets within a received input packet stream.

Amended claim 36 still further recites a "processor configured to fill a packet allocation table which includes a plurality of slot locations, each slot location storing the input port identifier from the packet header which identifies the input port that received the input packet stream to which a given packet belongs linked in the slot of the packet allocation table to an address in the memory for the addressable memory location where that given packet has been stored by the processor." The Examiner has previously pointed to the routing table in Chapman. However, Chapman does not teach filling a routing table with information wherein that information is the "input port identifier" taken "from the packet header" wherein that input port identifier "identifies the input port that received the input packet stream."

Additionally, Applicant points out that the Chapman routing table associates destination addresses of incoming packets to output ports. The claimed packet allocation table, on the other hand, associates (in each slot) "the input port identifier" for the input port receiving the packet and the "address in the memory for the addressable memory location where that given packet has been stored by the processor." The claimed invention is not met by Chapman. The Examiner's analysis of Chapman focuses on relationships between destination addresses read from the packet header and output port or delivery addresses. However, the packet header destination address is not the "input port identifier" claimed, and the delivery address is not the "address in the memory" where the packet is stored after receipt. The Examiner further points to Gaudet, but as discussed above Gaudet focuses on source port information, not the claimed input port identifier and its relationship to an address in memory where the packet is stored.

Amended claim 36 further recites "a destination pointer, associated with each one of the output ports, implemented by the processor and configured to point to a slot location in the packet allocation table from which the address of the given packet is retrieved, the destination pointer pointing to the slot location when the input port identifier in the slot matches the input port identifier mapped through the matrix to an output port associated with that destination pointer." The Examiner again points to the routing table in Chapman. While this routing table drives the routing operation in Chapman, that routing operation differs from the claimed invention in that the destination pointer of the claimed invention is pointed based on the

mapping relationship between the input port identifier and the output port as specified by the matrix. Chapman routes based on the relationship between the destination addresses read from the packet header and output port. There is no teaching or suggestion in Chapman for driving pointer operation based on an input port identifier and its association with one or more output ports.

The teachings of Gaudet and Wegner, which are also cited by the Examiner, do not suggest the claimed invention. Gaudet notes a source port identification within a packet header and Wegner teaches a queuing mechanism based on output port availability. Neither reference, however, teaching having the pointer for routing be assigned based on the stored relationship between the identifier of the input port where the packet was received and one or more output ports.

In view of the foregoing, Applicant submits that claim 36 is patentable over the cited prior art.

New claim 40 has been added. Claim 40 is asserted to be patentable over the cited prior art for at least the same reasons as claim 36.

Applicant respectfully submits that all claims of the application are in condition for favorable action and allowance.

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